

SCAN

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the application of:

Docket No.: 041-481-RB

Jorge Humberto Figueiredo

Group Art Unit: 2857

Serial No.: 09/531,860

Examiner: Jeffrey R. West

Filed: March 21, 2000

Date: January 5, 2004

Sent Via Fax (703) 746-7708

FOR: METHOD FOR TESTING MULTI-CHIP PACKAGES

SUPPLEMENTARY STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Per telephone conference this date with Examiner Jeffrey R. West, Applicant would now indicate his waiver (in the November 17, 2003 "Petition Under MPEP 601.01(d)") of the requested original filing date and will accept a later filing date as discussed.

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Also since there seemed to be some problem (with the Patent Office fax machine) in completely duplicating the allowed claim 10, Applicant is attaching another copy of claim 10 and now respectively requests a timely Notice of Allowance therefore.

Respectfully submitted,

Alfred W. Kozak

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CERTIFICATION UNDER 37 CFR 1.6(d)

I hereby certify that this document, and any other document herein referred to as enclosed, is being transmitted by facsimile to the U.S.PTO in accordance with 37 CFR 1.6(d) on the date given below.

Date:

January 5, 2004

Patti S. Preddy

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10. (Original) An apparatus for testing internal components of an integrated circuit package device under test to determine normal operation or problem areas in the components, said apparatus comprising:

- (a) test socket means for connecting the device under test with a digital multimeter in order to measure the power bus-to ground resistance of the internal components;
- (b) temperature transfer block means connected to a temperature meter for placement adjacent said device under test in order to increase the ambient heat or decrease the ambient heat to said device under test;
- (c) a Peltier-thermal electric module adjunct said transfer block means and connected to a programmable power supply for controlling the addition of heat to or reduction of heat from said temperature transfer block;
- (d) heat sink and fan means placed adjunct to said Peltier thermal electric module and connected to a controlled fan power supply;
- (e) computer means having a control program for connection and management of said controlled fan power supply, said programmable power supply and for sensing operations of said temperature meter and said digital multimeter to controllably enable the sequencing of an up-ramp temperature and a down ramp temperature adjacent said device under test, while concurrently reading-out and plotting the power bus-to ground voltage during the up-cycle and down-cycle of the temperature applied to said device under test.